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KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
BEHM, HARRY RAYMOND	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,801	FERGUSON, BRUCE R.	
	Examiner	Art Unit	
	Harry Behm	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 12-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka (US 6,157,182) in view of Farrenkof (US 6,229,293) and Shimamori (US 6,204,650).

3. With respect to Claim 1, Tanaka discloses a dual-mode pulse width modulation (PWM) buck converter, which operates in a hysteretic mode at low output currents and a continuous mode at high output currents. Tanaka does not disclose the use of pulse frequency modulation (PFM) nor does he disclose a boost converter where the current through the switch is sensed. The use of PFM techniques are widely known and taught by a number of sources including Bittner (US 5,568,044) and Shimamori (US 6,163,143). While Shimamori's implementation of the operation unit (Fig. 19 94) is digital, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the operation unit with analog circuitry because mappings between digital and analog circuits are well known in the art and analog implementations are often more economical when a microcomputer is not available. Shimamori teaches a pulse frequency modulator (Fig. 19 91) configured to control the switching

transistor, wherein the pulse frequency modulator is enabled during a burst period in which an output (Fig. 19 OUTPUT) of the power converter is less than a predetermined level (Fig. 19 REFERNCE VALUE). It would have been obvious to one of ordinary skill in the art at the time of the invention to replace the PWM controller of Tanaka with the PFM controller of Shimamori. The motivation to replace the PWM controller with the PFM controller would be to achieve higher efficiency; a PFM mode requires fewer turn-on transitions to maintain a constant output voltage than does a PWM mode of voltage regulation, thus resulting in a lower gate-drive power dissipation for PFM mode; further a PFM mode can be achieved with a much simpler control circuit having fewer components, thus the power dissipation in the control loop of a PFM mode is less than that of the control loop of a PWM mode. Farrenkopf teaches a boost converter (Fig. 1) with a switching transistor (Fig. 1 N1) and further discloses to sense the current through the switching transistor (Fig. 1 Rs). It also would have been obvious to one of ordinary skill in the art at the time of the invention to combine the dual-mode converter of Tanaka with the boost converter of Farrenkopf to create the invention claimed by Ferguson, the reason for doing so would be to obtain the benefit of an output voltage higher than the input voltage. Thus, the combined references teach a dual-mode (Tanaka Fig. 9 49) pulse frequency modulation (Shimamori Fig. 19 91,94) boost converter (Farrenkopf Fig. 1) comprising: a power conversion circuit that receives an input voltage at a first level (Farrenkopf Fig. 1 Vin) and that generates an output voltage at a second level (Farrenkopf Fi.

1 Vout), wherein the power conversion circuit includes a switching transistor (Farrenkopf Fig. 1 N1) to generate the output voltage; a pulse frequency modulator (Shimamori Fig 19 1,94) configured to control the switching transistor; an inner control loop (Tanaka Fig. 3 13) configured to sense a switching current (Farrenkopf Fig. 1 I_L) flowing through the switching transistor and to generate a first feedback signal (Tanaka Fig. 3 SECOND SIGNAL) to the pulse frequency modulator to turn the switching transistor (Farrenkopf Fig. 1 N1) off for a predefined duration (Shimamori Fig.19 92) when the switching current reaches a predetermined level (Tanaka Fig. 5 I_{LP}), wherein the predetermined level is substantially constant in a first mode (Tanaka "light load mode") and is controlled by an output voltage feedback signal (Tanaka Fig. 3 OUTPUT) in a second mode (Tanaka "heavy load mode"); and an outer control loop (Tanaka Fig. 3 12) configured to sense a load current (Tanaka Fig. 3 OUTPUT), wherein the output control loop turns the pulse frequency modulator off when the load current is greater than a reference level (Shimamori Fig. 19 96) during the first mode and forces the pulse frequency modulator to stay on during the second mode (Tanaka "heavy load mode") .

4. With respect to Claim 2, Tanaka teaches the invention as set forth above. He discloses a dual-mode switching regulator comprising: a switch (Farrenkopf Fig. 1 N1); a pulse frequency modulator (Shimamori Fig. 19 91,94) that controls switching cycles (Tanaka para 51 "current supply cycles") of the switch; and a first feedback loop (Tanaka Fig. 3 13) that detects when the switch conducts a

current above a selected threshold (Tanaka Fig. 5 I_{LP}) during each switching cycle and outputs a peak-current detection signal (Tanaka Fig. 3 SECOND SIGNAL) to the pulse frequency modulator in response to turn off the switch for a predefined duration (Shimamori Fig. 19 92), wherein the selected threshold is a substantially fixed threshold (Tanaka paragraph 5 "predefined reference level") in a first mode (Tanaka "light load mode") and a variable threshold (Shimamori Fig. 19 93) in a second mode (Tanaka "heavy load mode").

5. With respect to Claim 3, Tanaka discloses the dual-mode (Tanaka Fig. 9 49) switching regulator of Claim 2, further comprising a second feedback loop (Tanaka Fig. 3 12) that monitors an output (Tanaka Fig. 3 OUTPUT) of the dual-mode switching regulator for continuous closed-loop regulation and determines whether to operate the dual-mode switching regulator in the first mode (Tanaka "light load mode") or the second mode (Tanaka "heavy load mode"), wherein the second feedback loop outputs a burst control signal (Tanaka Fig. 3 FIRST SIGNAL) to turn on the pulse frequency modulator (Shimamori Fig. 19 91,94) for an active period during the second control signal mode or when the output (Farrenkopf Fig. 1 I_L) is less than a first level and to turn off the pulse frequency modulator when the output is greater than a second level (Shimamori Fig. 19 96).

6. With respect to Claim 4, Tanaka discloses the dual-mode switching regulator of Claim 2, wherein the dual-mode switching regulator is a boost converter (Farrenkopf Fig. 1) further comprising: an input inductor (Farrenkopf Fig. 1 L) coupled between an input voltage (Farrenkopf Fig. 1 Vin) and the switch

(Farrenkopf Fig. 1 N1); a rectifying diode (Farrenkopf Fig. 1 D) coupled between the input inductor and the output of the boost converter (Farrenkopf Fig. 1 Vout); and a filter capacitor (Farrenkopf Fig. 2 Cout) coupled between the output of the boost converter and ground.

7. With respect to Claim 5, Tanaka discloses the dual-mode switching regulator of Claim 3, wherein the second feedback loop (Tanaka Fig. 3 12) provides the variable threshold (Shimamori Fig. 19 93) to the first feedback loop (Tanaka Fig. 3 13), and the variable threshold is derived from the output (Farrenkopf Fig. 1 I_L) of the dual-mode switching regulator.

8. With respect to Claim 6, Tanaka discloses the dual-mode switching regulator of Claim 2, wherein the first mode is a hysteretic mode for relatively light load currents (Tanaka "light load mode") and the second mode is a continuous mode for relatively heavy load currents (Tanaka "heavy load mode").

9. With respect to Claim 7, Tanaka discloses the dual-mode switching regulator of Claim 3, wherein the second feedback loop (Tanaka Fig. 3 12) monitors the output voltage (Tanaka Fig. 3 OUTPUT) of the dual-mode switching regulator.

10. With respect to Claim 8, the dual-mode switching regulator of Claim 3, wherein the second feedback loop (Tanaka Fig. 3 12) monitors the peak-current detection signal (Tanaka paragraph 51 "current supply cycles") to switch operation (Tanaka Fig. 14) from the first mode (Tanaka "light load mode") to the second mode (Tanaka "heavy load mode") and monitors the variable threshold

(Shimamori Fig. 19 93) to switch operation (Tanaka Fig. 8) from the second mode to the first mode.

11. With respect to Claim 9, Tanaka discloses the dual-mode switching regulator of Claim 3, wherein the second feedback loop (Tanaka Fig. 3 12) switches the operation of the dual-mode switching regulator from the first mode (Tanaka "light load mode") to the second mode (Tanaka "heavy load mode") when the number of switching cycles (Tanaka paragraph 51 "current supply cycles") for the switch exceeds a predetermined value (Tanaka paragraph 51 "a controlling unit switches the operation from the light load mode to the heavy load mode so as to control the switch when the count value on the count unit exceeds a predetermined value") during an active period of the pulse frequency modulator.

12. With respect to Claim 10, Tanaka discloses the dual-mode switching regulator of Claim 7, wherein the second feedback loop switches (Tanaka Fig. 3 12) the operation of the dual-mode switching regulator from the second mode (Tanaka "heavy load mode") to the first mode (Tanaka "light load mode") when the variable threshold (Shimamori Fig. 19 93) is less than a predefined level. When the load current decreases to a level for the light load mode, the variable voltage also decreases and the mode is switched.

13. With respect to Claim 12, Tanaka teaches the invention as set forth above. He discloses a switching converter comprising: a semiconductor switch (Farrenkopf Fig. 1 N1); a pulse frequency modulation controller (Shimamori Fig.

19 91,94) configured to turn the semiconductor switch on and off; a peak current detector (Tanaka Fig. 3 13) configured to sense current flowing (Farrenkoph Fig. 1 I_L) through the semiconductor switch and to output a peak current pulse (Tanaka Fig. 3 SECOND SIGNAL) to the pulse frequency modulation controller (Shimamori Fig. 19 91,94) when the sensed current is above a reference peak level (Tanaka Fig. 5 I_{LP}), wherein the pulse frequency modulation controller turns off the semiconductor switch for a predetermined duration (Shimamori Fig. 19 92) in response to the peak current pulse; a feedback voltage detector (Tanaka Fig. 3 12) configured to sense an output voltage (Farrenkoph Fig. 1 Vout) of the switching converter and to output a control signal (Tanaka Fig. 3 FIRST SIGNAL) to the pulse frequency modulation switching controller wherein the control signal is in an active phase and turns on the pulse frequency modulation controller when the sensed output voltage is less than a first predefined voltage (Tanaka paragraph 5 "predefined reference value"), and wherein the control signal is in an inactive phase and turns off (Shimamori Fig. 19 96) the pulse frequency modulation controller when the sensed output voltage is greater than a second predefined voltage; and a load sensor configured to detect load current (Tanaka Fig. 3 12) and to output an override control signal to force the pulse frequency modulation controller to remain on (Shimamori Fig. 19 96) when the load current (Tanaka Fig. 3 OUTPUT) is greater than a predetermined level, wherein the reference peak level of the peak current detector (Tanaka Fig. 3 13) is a variable

peak level (Tanaka Fig. 5 I_{LP}) that varies with the sensed output voltage (Shimamori Fig. 19 Vout) when the override control signal is active.

14. With respect to Claim 13, Tanaka discloses the switching converter of Claim 12, wherein the reference peak level (Tanaka Fig. 5 I_{LP}) of the peak current detector is substantially constant when the override control signal (Tanaka Fig. 3 FIRST SIGNAL) is inactive.

15. With respect to Claim 14, Tanaka discloses the switching converter of Claim 12, wherein the variable peak level (Tanaka Fig. 5 I_{LP}) is generated by a filter circuit (Shimamori Fig. 19 95) coupled to an output of the feedback voltage detectors Vout).

16. With respect to Claim 15, Tanaka discloses the switching converter of Claim 14, further comprising a clamp circuit (Shimamori Fig. 19 96) coupled to an output of the filter circuit (Shimamori Fig. 19 95) to set the variable peak level (Tanaka Fig. 5 I_{LP}) at a predetermined value (Shimamori Fig. 19 93) when the override control signal (Tanaka Fig. 3 FIRST SIGNAL) is inactive.

17. With respect to Claim 16, Tanaka discloses the switching converter of Claim 12, wherein the feedback voltage detector (Tanaka Fig. 3 12) is a first comparator (Tanaka Fig. 8 31) with hysteresis (Shimamori Fig. 19 95) and the sensed output voltage (Shimamori Fig. 19 Vout) is provided to a negative input terminal of the first comparator while a first reference voltage (Shimamori Fig. 19 Vref) is provided to a positive input terminal of the first comparator.

18. With respect to Claim 17, Tanaka discloses the switching converter of Claim 12, wherein the load sensor further comprises: a counter (Tanaka Fig. 14 52) that increments with each peak current pulse (Tanaka paragraph 51 "current supply cycles") and resets (Tanaka Fig. 8 34) when the control signal is in the inactive phase; and a latch that sets (Tanaka Fig. 9 49) when the counter overflows (Tanaka Fig. 9 48) indicating that the load current (Tanaka Fig. 9 I_L) is greater than the predetermined level and resets (Tanaka Fig. 9 6) when the variable peak level is less than a predefined level indicating that the load current is less than the predetermined level.

19. With respect to Claim 18, Tanaka discloses the switching converter of Claim 16, wherein the load sensor is a second comparator (Tanaka Fig. 9 22) and the first reference voltage (Tanaka Fig. 9 V1) is provided to a positive input terminal of the second comparator while a second reference voltage (Tanaka Fig. 3 Vref) is provided to a negative input terminal of the second comparator.

20. With respect to Claim 19, Tanaka teaches the invention as set forth above. He discloses a method for improving efficiency of a switching regulator that uses pulse frequency modulation (Shimamori Fig. 19 92) to control a switch (Farrenkoph Fig. 1 N1), the method comprising the steps of: turning on a pulse frequency modulator for a burst period when an output (Tanaka Fig. 3 OUTPUT) of the switching regulator is less than a first level (Tanaka paragraph 51 "predetermined reference value"), wherein one or more switching cycles (Tanaka paragraph 51 "current supply cycles") for the switch occur in the burst period;

turning on the switch in each switching cycle until the switch conducts a peak current (Tanaka Fig. 5 I_{LP}) followed by a switch off-time of a predetermined duration (Shimamori Fig. 19 92); operating the switching regulator in a hysteretic mode for a first range of load currents (Tanaka "light load mode"), wherein the peak current for the switch is substantially fixed (Tanaka Fig. 5 I_{LP}) and the pulse frequency modulator turns off (Shimamori Fig. 19 96) when the output of the switching regulator is greater than a second level; and operating the switching regulator in a continuous mode for a second range of load currents (Tanaka "heavy load mode"), wherein the peak current for the switch (Tanaka Fig. 5 I_{LP}) varies according to a feedback signal indicative of an output (Farrenkoph Fig. 1 Vout) of the switching regulator and the pulse frequency modulator is forced on to extend the burst period until the variable peak current is less than a predefined level.

21. With respect to Claim 20, Tanaka discloses the method of Claim 19, wherein the switching regulator switches between operating modes (Tanaka Fig. 3 12) by indirect sensing of the load current (Tanaka Fig. 3 OUTPUT).

22. With respect to Claim 21, Tanaka discloses the method of Claim 19, wherein the switching regulator switches from the hysteretic mode to the continuous mode when the number of switching cycles in a burst period exceeds a predetermined value (Tanaka paragraph 51 "A count unit 32 counts the number of current supply cycles in the light load mode. A controlling unit 33 switches the operation mode from the light load mode to the heavy load mode so as to control

the switch unit 11 when the count value of the count unit 32 exceeds a predetermined value").

23. With respect to Claim 22, Tanaka discloses the method of Claim 19, wherein the switching regulator switches from the continuous mode to the hysteretic mode when the variable peak current is less than the predefined level (Tanaka paragraph 102 "when the load current decreases to a level for the light load mode, the operation mode is switched from the heavy load mode to the light load mode").

24. With respect to Claim 23, Tanaka discloses a switching regulator using a dual-mode pulse frequency modulation technique comprising: means for operating in a hysteretic mode (Tanaka Fig. 3 "light load mode"), wherein regulation of an output of the switching regulator is performed using a substantially fixed peak switching current (Tanaka Fig. 5 I_{LP}); and means for operating in a continuous mode (Tanaka "heavy load mode"), wherein regulation of the output of the switching regulator is performed using a variable peak switching current (Shimamori Fig. 19 93).

25. With respect to Claim 24, Tanaka discloses the switching regulator of Claim 23, further comprising means for sensing load power (Tanaka Fig. 9 Rsense) to switch between the hysteretic mode and the continuous mode (Tanaka Fig. 9 49).

26. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takata as applied to claim 2 above, and further in view of Bowman (6,791,283).

27. With respect to Claim 11, Tanaka discloses the dual-mode switching regulator of Claim 2, wherein the output (Farrenkopf Fig. 1 Vout) of the dual-mode switching regulator drives one or more light emitting diodes (Bowman Fig. 2 LED).

Conclusion

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Muratov (US 6,621,256) discloses a dual mode controller where a hysteretic control mode is selected when the measured current is sufficiently low. Bittner (US 5,568,044) discloses a dual mode PWM/PFM controller.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on business hours EST.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Gray can be reached on 571-272-2119. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Gray
Primary Examiner